IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Gary R. Gilliam	Examiner: Ernest F. Karlsen	
Serial No.:	09/935,232	Group Art Unit: 2829	
Filed:	August 22, 2001	Docket: 303.221US4	
Title:	ON-CHIP SUBSTRATE REGULATOR TEST MODE		

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

7# /amdt B, drwg. 12/23/02

Applicant has reviewed the Office Action mailed on August 26, 2002. Please amend the above-identified patent application as follows.

IN THE DRAWINGS

Enclosed is a copy of Figure 1 of the drawings showing the following proposed amendment to Figure 1 in red ink. A block diagram of a DRAM memory device 100 is included with an array of memory cells 110. Applicant notes that page 1, lines 11-12 of the specification as filed provides support for embodiments of the invention incorporated into a memory device. Applicant respectfully submits that one of ordinary skill in the art will appreciate that memory devices include DRAM devices and arrays of memory cells 110 as included in Figure 1.

Applicant respectfully submits that no new matter has been added as a result of the proposed amendments to Figure 1. Reconsideration and withdrawal of the objections to the drawings is respectfully requested.

IN THE SPECIFICATION

Please make the paragraph substitutions indicated in the appendix entitled Clean Version of Amended Specification Paragraphs. The specific changes incorporated in the substitute paragraphs are shown in the following marked-up versions of the original paragraphs:

The paragraph beginning on page 2, line 24, is amended as follows:

In one embodiment of Figure 1, a memory device 100 such as a DRAM memory device is shown having an array of memory cells 110. The invention is, however not limited to embodiments that include a memory device. Referring to Figure 1, Vcc is a supply voltage level.